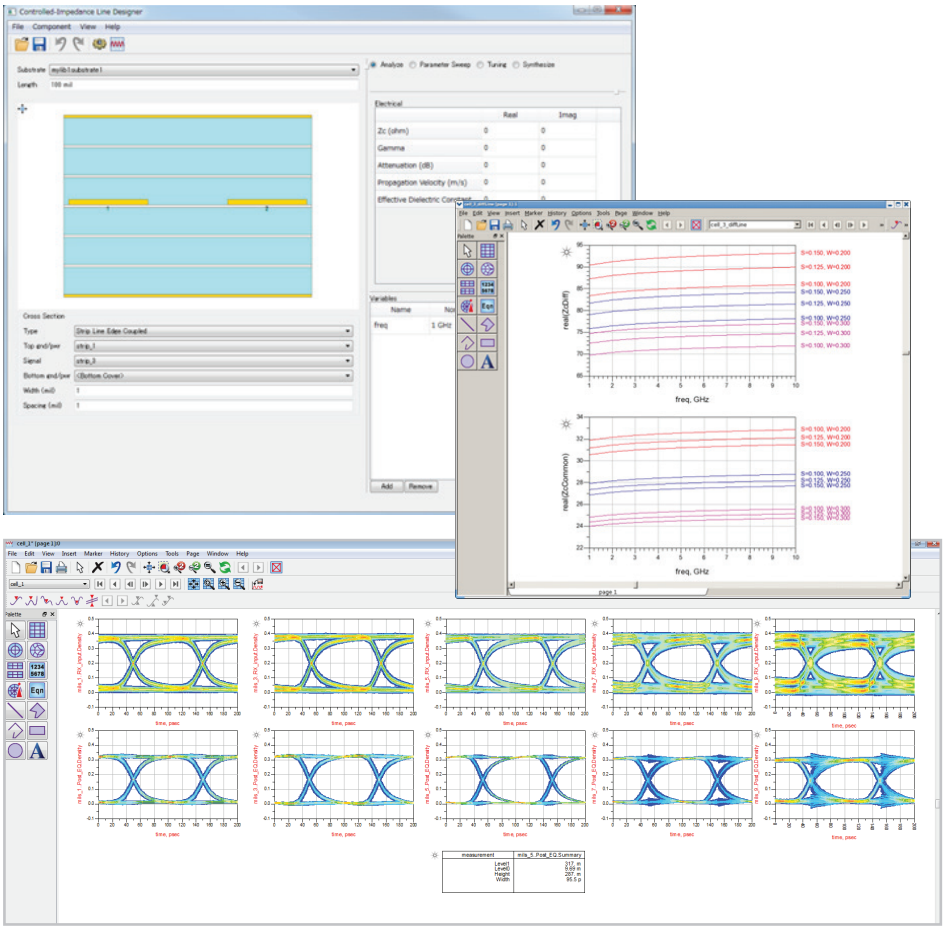
Keysight W2307EP/ET
Controlled Impedance Line Designer (CILD)

Data Sheet

Controlled Impedance Line Designer lets you optimize your PCB stack up and transmission line geometry using metrics that matter, namely post-equalizer eye diagram parameters. Other tools will show you the impairments of the lines, such as loss, frequency roll off, and impedance variation, but in today's multi gigabit chip to chip links these metrics are inadequate. What really matters is the eye parameters after the line impairments have been mitigated by the signal processing in modern SerDes, for example Tx pre-emphasis and Rx equalization. In fact the whole point of the signal processing in the I/O of modern chips is to allow you to use lower cost materials and yet still open the eye.

Controlled Impedance line Designer achieves this by letting you place a Tx and Rx around the candidate line to form a complete ADS Channel Simulator or ADS Transient Simulator schematic. In particular, the statistical mode of Channel Simulator can yield ultra low BER contours in seconds per point in the design space. You can quickly sweep parameters like width and spacing to see the effect.



Key Features

- Create a pre-layout channel in an end-to-end ADS Channel Simulator schematic
- Optimize the metrics that matter
  - Eye Diagram parameters including mitigation
  - Bode plots of the channel impairment
- Design the stack up and line geometry of the controlled impedance lines
- Determine the parameters that you feed into the Constraint Manager of the auto-router in your enterprise PCB tool

Requirements

- OS platform support: Linux 64-bit Windows 64-bit
- W2200 ADS Core
- W2302 ADS Transient Convolution Simulator Element : only required if line is to be evaluated in a end-to-end simulation

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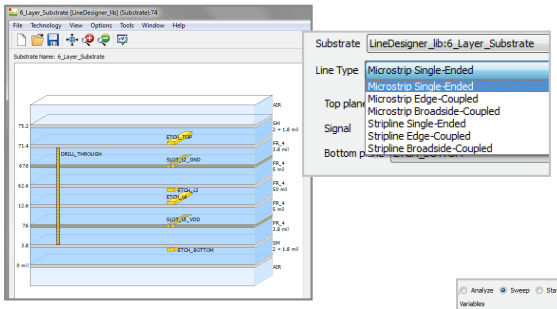
Steps For Characterizing Your Pre-Layout Design

The starting point is a Technology Substrate. CILD can be used to characterize the physical parameters of the transmission line, substrate thicknesses, and material parameter values so you obtain the desired characteristic impedance for the line. The parameters that result from a CILD analysis can be transferred to ADS as a Technology Line Type. Such Line Type can then be used in a pre-layout schematic. The new LTLINE components make a reference to the line type. Likewise, in layout, the Line Type can be referenced from an LTLINE component or from the new Route interconnect object.

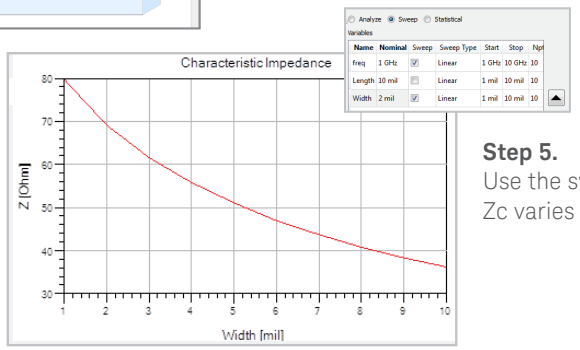
Step 1.
Open your multi-layer substrate design in the ADS substrate editor

Step 2.
Select Tools > Controlled Impedance Line Designer to open CILD

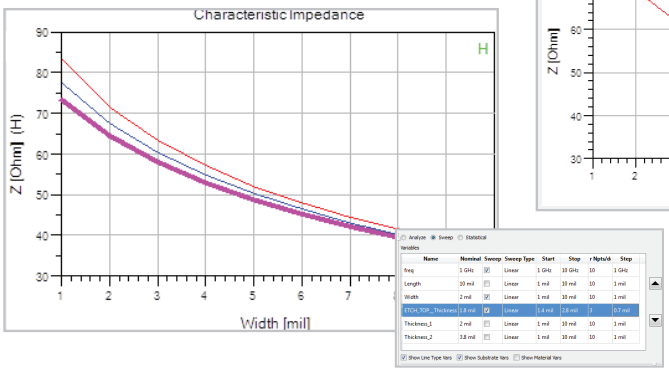


Step 3.
Select a microstrip line to characterize and define the cross-section of the transmission line

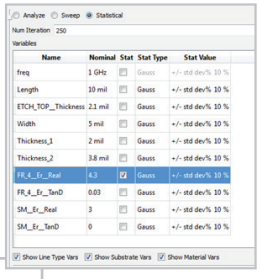
Step 4.
Run the simulation and analyze the results



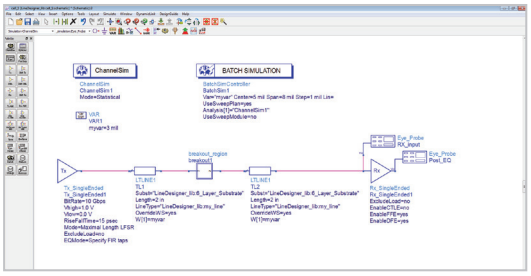
Step 5.
Use the sweep analysis to see how the Zc varies versus the width of the line



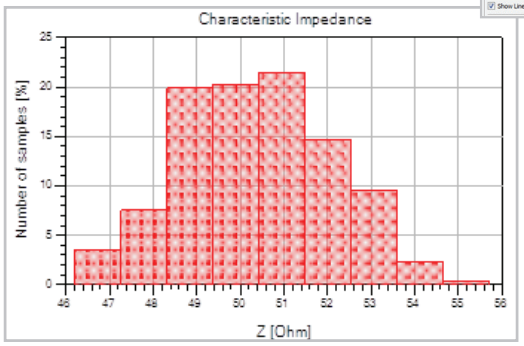
Step 6.
Investigate how Zc changes versus the thickness of the conductor



Step 7.
Use the statistical analysis mode to characterize the sensitivity of your design



Step 8.
Update your CILD Substrate/Material Parameter results in ADS



Step 9.
All parameters linked to the cross-section of the line can be used to define a new or update an existing Line Type

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